Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary		Application No.	Applicant(s)
		09/961,024	MEARS ET AL.
		Examiner	**Art Unit**	
		Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>12 August 2004</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-48</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-48</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>21 September 2001</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date <u>20030403</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   There are some errors in the applicant's amendment filed on August 12, 2004. Claims 14-15 are

dependent claims; but they are referred to as independent claims in the remarks. Claim 19 has some

limitations that are indicated as amended; but only the word "control" has been amended in the original

claim.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

3.   Claims 45-48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the

written description requirement. The claim(s) contains subject matter which was not described in the

specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s),

at the time the application was filed, had possession of the claimed invention. The specification does not

disclose the method of providing null data when selected channel register is empty in claim 45. The

specification also does not disclose the method of applying a strobe signal when null data is provided in

claim 46.

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

5.   Claims 19-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6.   Claim 19 is rejected because the claim language is unclear. The claim recites "wherein each of

the first and second communications interface include: a bus interface coupled to the first semiconductor

chip." The drawings do not show the second communications interface being coupled to the first

semiconductor chip.

7.   Claims 20-27 are rejected since they are dependent on rejected claims 19.

Drawings

8.   The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of

the invention specified in the claims. Therefore, the second communications interface includes a bus

interface coupled to the first semiconductor chip must be shown or the feature(s) canceled from the

claim(s). No new matter should be entered.

        Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing sheet should include

all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being

amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a

drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and

where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

description of the several views of the drawings for consistency. Additional replacement sheets may be

necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will

not be held in abeyance.

Claim Rejections - 35 USC § 102

9.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis

for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10.   Claims 1-2 and 36 are rejected are under 35 U.S.C. 102(b) as being anticipated by Holm et al.('680), hereinafter referred to as Holm.

11.   Regarding claim 1, Holm discloses a communications interface, comprising: a bus interface(Figure 1, 30-33) coupleable to an internal bus(Figure 1, 60 and 62), a plurality of transmit channels coupled to the bus interface(Figure 1, 70-73); a transmit control block(Figure 1, 40) coupled to the plurality of transmit channels; a plurality of outbound links coupled to a plurality of outputs of the transmit control block(Figure 1, 50); a plurality of receive channels coupled to the bus interface(Figure 1, 80-83); and a receive control block(Figure 1, 42) coupled to the plurality of receive channels; and a plurality of inbound links coupled to a plurality of inputs of the receive control block(Figure 1, 52), the inbound links and the outbound links to couple the bus interface to a further bus interface(Column 2, Lines 35-40; It is inherent a further bus interface is connected to the links).

12.   Regarding claim 2, Holm discloses a communications interface, further comprising a direct memory access controller(Figure 1, 44) coupled to the bus interface.

13.   Regarding claim 36, Holm discloses a method of forming a communications interface, comprising: forming a bus interface(Figure 1, 30-33); forming a plurality of transmit channels coupled to the bus interface(Figure 1, 70-73); forming a transmit control block(Figure 1, 40) coupled to the plurality of transmit channels; forming a plurality of outbound links coupled to a plurality of outputs of the transmit control block(Figure 1, 50); forming a plurality of receive control channels coupled to the bus interface(Figure 1, 80-83); forming a receive control block(Figure 1, 42) coupled to the plurality of

receive control channels; and forming a plurality of inbound links coupled to a plurality of inputs of the

receive control block((Figure 1, 52)), the inbound links and the outbound links to couple the bus interface

to a further bus interface(Column 2, Lines 35-40; It is inherent a further bus interface is connected to the

links).

14.   Claims 1-13, 16-18, and 36-44 are rejected are under 35 U.S.C. 102(e) as being anticipated by

Baker('938).

15.   Regarding claim 1, Baker discloses a communications interface, comprising: a bus

interface(Figure 2, 104) coupleable to an internal bus, a plurality of transmit channels coupled to the bus

interface(DMA channels); a transmit control block coupled to the plurality of transmit channels(Figure 2,

78 and 90 combined); a plurality of outbound links coupled to a plurality of outputs of the transmit

control block(Figure 1, 16); a plurality of receive channels coupled to the bus interface(DMA channels);

and a receive control block(Figure 2, 78 and 90 combined) coupled to the plurality of receive channels;

and a plurality of inbound links coupled to a plurality of inputs of the receive control block(Figure 1, 16),

the inbound links and the outbound links to couple the bus interface to a further bus interface(Figure 1,

18).

16.   Regarding claim 2, Baker discloses a communications interface, further comprising a direct

memory access controller(Figure 2, 72) coupled to the bus interface.

17.   Regarding claim 3, Baker discloses a communications interface, wherein the bus interface

comprises a plurality of transmit control registers and a plurality of receive control registers(Figure 2, 88).

18.   Regarding claim 4, Baker discloses a communications interface, wherein the plurality of transmit

control registers comprises a transmit first in first out (FIFO) register associated with each transmit

channel(Figure 2, 82, 84) and a channel status register associated with each transmit channel(Figure 2,

88).

19.   Regarding claim 5, Baker discloses a communications interface, wherein the plurality of receive control registers comprises a receive FIFO register coupled to each receive channel(Figure 2, 80) and a channel status register associated with each receive channel(Figure 2, 88).

20.   Regarding claim 6, Baker discloses a communications interface, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises a first in first out (FIFO) memory device(Figure 2, 80, 82, 84).

21.   Regarding claim 8, Baker discloses a communications interface, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated(Figure 12, 340).

22.   Regarding claim 9, Baker discloses a communications interface, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel across a selected link.(Figure 2, 90).

23.   Regarding claim 10, Baker discloses a communications interface, wherein the receive control block comprises a state machine adapted to store a current active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels(Figure 12, 352; Column 13, Lines 12-14).

24.   Regarding claim 11, Baker discloses a communications interface, wherein the plurality of transmit channels comprises: at least one channel adapted to send a clock signal(Figure 26b, clkA); at least one channel adapted to send a strobe signal(Figure 12, 356); at least one channel adapted to send a wait signal(Column 26, Lines 40-41); and at least one channel adapted to send data(Column 26, Lines 66-67).

25.   Regarding claim 12, Baker discloses a communications interface, wherein the plurality of receive channels comprises: at least one channel adapted to send a clock signal(Figure 26b, clkB); at least one

channel adapted to send a strobe signal(Figure 12, 356); at least one channel adapted to send a wait

signal(Column 25, Lines 20-23); and at least one channel adapted to send data(Column 25, Lines 28-29).

26.   Regarding claim 13, Baker discloses a communications interface, wherein at least one of the

plurality of transmit channels and the plurality of receive channels comprise a virtual general purpose

input/output channel(Column 7, Lines 42-43).

27.   Regarding claim 16, Baker does discloses at least one of a direct flow control mode and a

message flow control to control a flow of data across the communications interface(Column 19, Lines 7-

15).

28.   Regarding claim 17, Baker discloses a communications interface, wherein the transmit control

block comprises: a multiplexer coupled to the plurality of transmit channels; a parallel in serial out

converter (PISO)(Column 6 Lines 20-22) coupled to the multiplexer; and a control circuit coupled to the

multiplexer and the PISO and adapted to select one of the plurality of transmit channels to transmit

data(Fig 12, 344).

29.   Regarding claim 18, Baker discloses a communications interface, wherein the receive control

block comprises: a demultiplexer coupled to the plurality of receive channels; a serial in parallel out

converter (SIPO)(Column 6 Lines 20-22); and a control circuit coupled to the demultiplexer and adapted

to select one of the plurality of receive channels to receive data((Fig 12, 344).

30.   Regarding claim 36, Baker discloses a method of forming a communications interface,

comprising: forming a bus interface(Figure 2, 104), forming a plurality of transmit channels coupled to

the bus interface(DMA channels); forming a transmit control block coupled to the plurality of transmit

channels(Figure 2, 78 and 90 combined); forming a plurality of outbound links coupled to a plurality of

outputs of the transmit control block(Figure 1, 16); forming a plurality of receive channels coupled to the

bus interface(DMA channels); forming a receive control block(Figure 2, 78 and 90 combined) coupled to

the plurality of receive channels; and forming a plurality of inbound links coupled to a plurality of inputs

of the receive control block(Figure 1, 16), the inbound links and the outbound links to couple the bus

interface to a further bus interface(Figure 1, 18).

31.   Regarding claim 37, Baker discloses a method, wherein forming the bus interface comprises

forming a plurality of transmit control registers and a plurality of receive control registers((Figure 2, 88).

32.   Regarding claim 38, Baker discloses a method, wherein forming the transmit control block

comprises: forming a channel arbiter adapted to determine a next one of the plurality of channels to be

activated(Figure 12, 340); and forming a link controller adapted to transmit data from a selected transmit

channel across a selected link(Figure 2, 90).

33.   Regarding claim 39, Baker discloses a method, wherein forming the receive control block

comprises forming a state machine adapted to store a currently active channel number, a number of bits in

a current byte being transferred and to write each byte to a selected one of the plurality of receive

channels(Figure 12, 352; Column 13, Lines 12-14).

34.   Regarding claim 40, Baker discloses a method, wherein forming the plurality of transmit channels

and forming the plurality of receive channels, each comprises: forming at least one channel adapted to

send a clock signal(Figure 26b, clkA, clkB); forming at least one channel adapted to send a strobe

signal(Column 12, 356); forming at least one channel adapted to send a wait signal(Column 26, Lines 40-

41; Column 25, Lines 20-23); and forming at least one channel adapted to send data(Column 25, Lines

28-29; Column 26, Lines 66-67).

35.   Regarding claim 41, Baker discloses a method, further comprising forming at least one virtual

general purpose input/output channel(Column 7, Lines 42-43).

36.   Regarding claim 42, Baker discloses a method, wherein forming the transmit control block

comprises: forming a multiplexer coupled to the plurality of transmit channels; forming a parallel in serial

out converter (PISO)(Column 6, Lines 20-22) coupled to the multiplexer; and forming a control circuit

coupled to the multiplexer and to the PISO(Figure 12, 344).

37.   Regarding claim 43, Baker discloses a method, wherein forming the receipt control block

comprises: forming a demultiplexer coupled to the plurality of receive channels; forming a serial in

parallel out converter (SIPO)(Column 6; Lines 20-22); forming a control circuit coupled to the

demultiplexer and adapted to select one of the plurality of receive channels to receive data(Figure 12,

344).

38.   Regarding claim 44, Baker discloses a method comprising: supplying a clock signal from a first

terminal; supplying a strobe signal from a second terminal; providing an identification value

corresponding to a selected channel register from data terminals when the strobe signal is active;

providing data from the selected channel register at the data terminals when the strobe signal is inactive,

the data changing in accordance with the clock signal; and providing a third terminal that receives a wait

signal that keeps the data provided at the data terminals from changing(Figure 12, Column 17, Lines 34-

50).

Claim Rejections - 35 USC § 103

39.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

40.   This application currently names joint inventors. In considering patentability of the claims under

35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly

owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of

each claim that was not commonly owned at the time a later invention was made in order for the examiner

to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under

35 U.S.C. 103(a).

41.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baker, in view of what is well known in the art.

42.   Baker does not specifically disclose a power management unit coupled to each of the plurality of transmit channels and receive channels. However, Official Notice is being taken that advantages of power management are well known in the art. Therefore, it would have been obvious to include a power management unit in the system of Baker since this would allow power to be saved during periods of inactivity

43.   Claims 14-15 and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker, in view of Earnest('338).

44.   Regarding claim 14, Baker discloses a communications interface, further comprising: a start threshold register adapted to set a start threshold value to cause a start message to be sent to a source when the receive FIFO can receive additional data(Column 19, Lines 7-15).

        Baker does not disclose a channel stop threshold register adapted to set a threshold value to cause a stop message to be sent to a source when a receive FIFO is full. However, Earnest discloses a stop threshold register adapted to set a threshold value to cause a stop message to be sent to a source when a receive FIFO is full(Column 11, Lines 40-45). Therefore, it would have been obvious to include the stop threshold register, as disclosed by Earnest, in the system of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

45.   Regarding claim 15, Baker discloses a communications interface, further comprising: a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value(Column 19, Lines 7-15).

        Baker does not disclose a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value. However, Earnest discloses a stop message channel coupled to the receive control block and adapted to send a stop message

to a source when a receive FIFO reaches a stop threshold value(Column 11, Lines 40-45). Therefore, it

would have been obvious to include the stop message channel, as disclosed by Earnest, in the system of

Baker, since this would prevent the writing of data in FIFO that has no more room for data.

46.   Regarding claim 28, Baker discloses a method of transmitting data between semiconductor chips,

comprising writing data into at least one of a plurality of transmit FIFOs(Figure 2, 82, 84); selecting one

of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait

state(Column 14, Lines 20-28; Column 18, Lines 58-60).

    Baker does not disclose and transmitting the data to a corresponding one of the plurality of

receive FIFOs that has not exceeded a threshold value. However, Earnest discloses and transmitting the

data to a corresponding one of the plurality of receive FIFOs that has not exceeded a threshold

value(Column 11, Lines 40-45). Therefore, it would have been obvious the teachings of Earnest, with that

of Baker, since this would prevent the writing of data in FIFO that has no more room for data.

47.   Regarding claim 29, Baker discloses a method, further comprising: sending a wait signal to a

transmit control block if the corresponding one of the receive FIFOs cannot receive data; and removing

the wait signal when the corresponding one of the receive FIFOs can receive data(Column 26, Lines 40-

41).

48.   Regarding claim 30, Baker discloses a method, further comprising selecting another one of the

plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs

while the corresponding one of the receive FIFOs cannot receive data(Column 14, Lines 20-28).

49.   Regarding claim 31, Baker discloses a method, further comprising: sending a strobe signal to

initiate a transmission of data(Figure 12, 356); sending a selected channel number over which the data is

to be transmitted(Column 14, Lines 20-28); and sending an end of message signal after the data has been

transmitted(Column 25, Lines 62-64).

50.   Regarding claim 32, Baker discloses a method, further comprising: sending a start message when the corresponding one of the receive FIFOs can receive data(Column 19, Lines 7-15). Earnest discloses sending a stop message if the corresponding one of the receive FIFOs cannot receive data(Column 11, Lines 40-45).

51.   Regarding claim 33, Baker discloses a method, further comprising: selecting one of the plurality of transmit FIFOs and the corresponding one of the plurality of receive FIFOs by a predetermined algorithm(Figure 13).

52.   Regarding claim 34, Baker does not disclose the predetermined algorithm is round-robin. However, the round-robin algorithm is a well-known arbitration scheme and therefore could be substituted for the arbitration scheme in Baker's system.

53.   Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baker, in view of Earnest, and in further view of Holm.

        Baker and Earnest does not disclose a method, further comprising selecting an interface width from one of a serial width, a two-bit width and a nibble width. However, Holm discloses width of the data bus being any size(Column 8, Lines 31-32). Therefore it would have been obvious to use the teachings of Holm in the system of Baker and Earnest, to use a bus with varying width since this would increase compatibility.

Response to Arguments

54.   Applicant's arguments with respect to claims 1-27 and 35-43 have been considered but are moot in view of the new ground(s) of rejection.

55.   Applicant's arguments regarding claims 14-15 and 28-34, filed August 8 2004 have been fully considered but they are not persuasive. Applicant argues that Baker does not show the limitation "when not in a wait state" in claim 28. However, as stated in the rejection above, Baker discloses transmitting

data from a FIFO that is not in a wait state. Applicant further argues that no reasoning was included for

the motivation to combine the references of Baker and Earnest in the rejection of claims 14-15. However,

as stated in the rejection above, reasoning for the combination of references has been included, i.e. to

prevent further writing in a FIFO that is already full.

Conclusion

56.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office

action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is

reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from

the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing

date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX

MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Nimesh G Patel whose telephone number is 571-272-3640. The examiner can normally be

reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark

H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
October 29, 2004

Glenn A. Auve
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